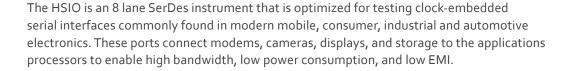


Diamond_x HSIO

8 Lane SerDes Instrument for Testing of High-Speed Serial Interfaces







Automotive



Consume



Flat Panel Display



IoT/IoV & Optoelectronics

Industrial & Medical



MCU



Mobility

Highlights

- Physical layer testing with built in PRBS BERTTX/RX
- BIST/DFT testing using high bandwidth drive/compare memory
- Protocol level testing using deep send and receive pattern memories

Features

- Test of high speed serial ports with data rates up to 6.4 Gpbs, such as HDMI, MIPI, JESD204, PClexpress, SATA, EDP
- 8 differential, split I/O lanes, configured as two 4 lane ports
- Hardware clock data recovery per lane with flexible BERT sync
- Deep source and capture memory, as well as built in PRBS and 8b/10b encoding
- Per wire PMU for DC parametrics and common mode shift capability

- SerDes
- 8 differential TX channels
- 8 RX Differential Channels

- 6.4 Gb Data Rate
- 128M TX Vector Memory Jitter Injection
- Eye Mask, PRBS



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Specifications

Channels		Transmitter	
Channels per instrument	8 Differential TX, 8 Differential RX	 Driver Min/Max Level range – DC Coupled 	o to 1.5V
Frequency Specifications		 Driver Swing range 	0.1 to 1.5V
 Time Domains per Instrument	2, one time domain per 4 lanes	 AC Coupled Termination Voltage Range 	o to 3.5V
• UI period	156.25 ps to 10000 ps (100 Mbps to 6.4 Gpbs)	• Eye Opening at 6.4 Gbps	60% minimum
 On-the-fly Period Change Range 	2 to 62, Even integer division of primary rate	 Programmable Pre-Emphasis Amplitude 	30 %
Operating Modes		 Jitter Injection Range 	+/-40UI
• DUT Phy Mode (PRBS, BIST)	8 inputs and 8 outputs; up to 24oK bit cell pattern depth, force and expect only	Pattern Specifications	
		Clocking Mode	Embedded Clock
		Differential Input Impedance	100 Ω
• DUT RX mode	8 inputs; up to 128M symbols	Minimum Edge Density	1 transition per 4096 UI
• DUTTX mode	8 outputs; up to 128M symbols	 Minimum Bit Lock Transitions 	8192 transitions
		 Tracking Loop Bandwidth 	1 MHz
DUT Duplex mode	4 inputs and 4 outputs; up to 128M symbols, force and	• Lane-Lane Deskew Range	1000 UI
	expect or force and capture	• Input Level Range	o to 1.5 V
Pattern Specifications	Cto co CIII mondulo c	 Min/Max Input Amplitude 	5 mV to 1.5 V
Keepalive Memory Size	16 to 4096 UI, modulo 4 increments	AC Coupled Input Voltage Range	o to 3.5 V
Built-In PRBS BERT	PRBS 7, 15, 23 or 31	 Vref Range 	o to 1.5 V
 PRBS Seed Value 	1 to 2n+1-1	Receiver Equalization	31 % ti 74 %
 History RAM 	256 symbols	Minimum Eye Opening Required	30 %
Pattern Key Match Word	40 bits	at 6.4 Gbps	J • / •

All specifications are subject to change without notification and are for reference only. For detailed performance specifications, please contact Cohu.

PPMU

• Voltage Range

Current Ranges

-1.2 V to 3.5 V

+/-8 t, +/-32 mA

• Sync/Training Key Word

• Out of Band Signaling

Disparity

10 bits

on/off

control

Transmit on/off, Receive

On/off under pattern